CURRENT CLAIMS

A copy of the claims is provided for the convenience of the Examiner. The claims are not amended.

1. (Previously Presented) A phase-locked loop (PLL) frequency synthesizer comprising:

a voltage controlled oscillator (VCO) that receives a frequency control voltage level stored on a loop filter and generates an output clock signal having an operating frequency, Fout, determined by said frequency control voltage level;

a first frequency divider for dividing said operating frequency, Fout, of said output clock signal by a first divider value, N, to produce a first divided clock signal having a frequency, Fout/N;

a second frequency divider for dividing a reference frequency, Fin, of an incoming reference clock signal by a second divider value, M, to produce a second divided clock signal having a frequency, Fin/M;

a phase-frequency detector capable of comparing said first and second divided clock signals and generating an UP control signal if said first divided clock signal is slower than said second divided clock signal and generating a DOWN control signal if said first divided clock signal is faster than said second divided clock signal;

a charge pump capable of receiving said UP and DOWN control signals and increasing said frequency control voltage level on said loop filter by injecting a charge pump current, Ic,

and decreasing said frequency control voltage level on said loop filter by draining said charge pump current, Ic; and

a loop response control circuit capable of adjusting a value of Ic as a function of said first divider value, N, and said second divider value, M, wherein said loop response control circuit is capable of adjusting the value of Ic based at least partially on at least one of: one of a first plurality of ranges in which said first divider value lies and one of a second plurality of ranges in which said second divider value lies.

2. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 1 wherein said loop response control circuit, for a given value of M, sets Ic to a minimum current level when N is in the range $1 \leq N \leq K$ and sets Ic to a second current level higher than said minimum current level when N is in the range $K+1 \leq N \leq P$.

3. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 2 wherein said second current level is approximately twice said minimum current level.

4. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 3 wherein said loop response control circuit sets Ic to a third current level higher than said second current level when N is in the range $P+1 \leq N \leq S$.

5. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 4 wherein said third current level is approximately twice said second current level.

6. (Previously Presented) The phase-locked loop frequency synthesizer as set forth in Claim 1 wherein said loop response control circuit, for a given value of N, sets Ic to a maximum current level when M is in the range $1 \leq M \leq J$ and sets Ic to a second current level lower than said maximum current level when M is in the range $J+1 \leq M \leq Q$.

7. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 6 wherein said second current level is approximately one half of said maximum current level.

8. (Previously Presented) The phase-locked loop frequency synthesizer as set forth in Claim 7 wherein said loop response control circuit sets Ic to a third current level lower than said second current level when M is in the range $Q+1 \leq M \leq T$.

9. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 8 wherein said third current level is approximately one half of said second current level.

10. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 1 wherein said loop response control circuit is further capable of adjusting a resistance, R, of a filter resistor associated with said loop filter as a function of said first divider value, N, and said second divider value, M.

11. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 10 wherein said loop response control circuit, for a given value of N, sets R to a minimum resistance value when M is in the range $1 \leq M \leq U$ and sets R to a second resistance level higher than said minimum resistance level when M is in the range $U+1 \leq M \leq V$.

12. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 11 wherein said second resistance level is approximately twice said minimum resistance level.

13. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 12 wherein said loop response control circuit sets R to a third resistance level higher than said second resistance level when M is in the range $V+1 \leq M \leq W$.

14. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 13 wherein said third resistance level is approximately twice said second resistance level.

15. (Previously Presented) An integrated circuit comprising:

a processor capable of operating at a plurality of clock speeds;

a phase-locked loop (PLL) frequency synthesizer capable of providing at least one clock signal having a variable clock speed to said processor, said PLL frequency synthesizer comprising:

a voltage controlled oscillator (VCO) that receives a frequency control voltage level stored on a loop filter and generates an output clock signal having an operating frequency, Fout, determined by said frequency control voltage level;

a first frequency divider for dividing said operating frequency, Fout, of said output clock signal by a first divider value, N, to produce a first divided clock signal having a frequency, Fout/N;

a second frequency divider for dividing a reference frequency, Fin, of an incoming reference clock signal by a second divider value, M, to produce a second divided clock signal having a frequency, Fin/M;

a phase-frequency detector capable of comparing said first and second divided clock signals and generating an UP control signal if said first divided clock signal is slower than said second divided clock signal and generating a DOWN control signal if said first divided clock signal is faster than said second divided clock signal;

a charge pump capable of receiving said UP and DOWN control signals and increasing said frequency control voltage level on said loop filter by injecting a charge pump current, Ic, and decreasing said frequency control voltage level on said loop filter

by draining said charge pump current, Ic; and

a loop response control circuit capable of adjusting a value of Ic as a function of said first divider value, N, and said second divider value, M, wherein said loop response control circuit is capable of adjusting the value of Ic based at least partially on at least one of: one of a first plurality of ranges in which said first divider value lies and one of a second plurality of ranges in which said second divider value lies.

16. (Original) The integrated circuit as set forth in Claim 15 wherein said loop response control circuit, for a given value of M, sets Ic to a minimum current level when N is in the range $1 \leq N \leq K$ and sets Ic to a second current level higher than said minimum current level when N is in the range $K+1 \leq N \leq P$.

17. (Original) The integrated circuit as set forth in Claim 16 wherein said second current level is approximately twice said minimum current level.

18. (Original) The integrated circuit as set forth in Claim 17 wherein said loop response control circuit sets Ic to a third current level higher than said second current level when N is in the range $P+1 \leq N \leq S$.

19. (Original) The integrated circuit as set forth in Claim 18 wherein said third current level is approximately twice said second current level.

20. (Previously Amended) The integrated circuit as set forth in Claim 15 wherein said loop response control circuit, for a given value of N, sets Ic to a maximum current level when M is in the range $1 \leq M \leq J$ and sets Ic to a second current level lower than said maximum current level when M is in the range $J+1 \leq M \leq Q$.

21. (Original) The integrated circuit as set forth in Claim 20 wherein said second current level is approximately one half of said maximum current level.

22. (Previously Presented) The integrated circuit as set forth in Claim 21 wherein said loop response control circuit sets Ic to a third current level lower than said second current level when M is in the range $Q+1 \leq M \leq T$.

23. (Original) The integrated circuit as set forth in Claim 22 wherein said third current level is approximately one half of said second current level.

24. (Original) The integrated circuit as set forth in Claim 15 wherein said loop response control circuit is further capable of adjusting a resistance, R, of a filter resistor associated with said loop filter as a function of said first divider value, N, and said second divider value, M.

25. (Original) The integrated circuit as set forth in Claim 24 wherein said loop response control circuit, for a given value of N, sets R to a minimum resistance value when M is in the range $1 \leq M \leq U$ and sets R to a second resistance level higher than said minimum resistance level when M is in the range $U+1 \leq M \leq V$.

26. (Original) The integrated circuit as set forth in Claim 25 wherein said second resistance level is approximately twice said minimum resistance level.

27. (Original) The integrated circuit as set forth in Claim 26 wherein said loop response control circuit sets R to a third resistance level higher than said second resistance level when M is in the range $V+1 \leq M \leq W$.

28. (Original) The integrated circuit as set forth in Claim 27 wherein said third resistance level is approximately twice said second resistance level.

29. (Previously Presented) A circuit, comprising:

a first frequency divider capable of dividing a frequency of an output clock signal based on a first divider value, the output clock signal produced by a voltage controlled oscillator;

a second frequency divider capable of dividing a frequency of a reference clock signal based on a second divider value;

a charge pump capable of generating a charge pump current based on an output of the first frequency divider and an output of the second frequency divider, the charge pump current altering a frequency control voltage level used by the voltage controlled oscillator to generate the output clock signal; and

a loop response control circuit capable of adjusting the charge pump current based at least partially on at least one of: one of a first plurality of ranges in which the first divider value lies and one of a second plurality of ranges in which the second divider value lies.

30. (Previously Presented) The circuit of Claim 29, wherein the first plurality of ranges comprises ranges of $1 \leq N \leq 8$, $9 \leq N \leq 16$, $17 \leq N \leq 32$, $33 \leq N \leq 64$, and $65 \leq N \leq 128$, where N represents the first divider value.

31. (Previously Presented) The circuit of Claim 30, wherein the loop response control circuit is capable of doubling the charge pump current when the first divider value moves from one of the first plurality of ranges into a next higher one of the first plurality of ranges.

32. (Previously Presented) The circuit of Claim 29, wherein the second plurality of ranges comprises ranges of $1 \leq M \leq 4$, $5 \leq M \leq 8$, and $9 \leq M \leq 16$, where M represents the second divider value.

33. (Previously Presented) The circuit of Claim 32, wherein the loop response control circuit is capable of reducing the charge pump current by half when the second divider value moves from one of the second plurality of ranges into a next higher one of the second plurality of ranges.

34. (Previously Presented) The circuit of Claim 29, further comprising a phase-frequency detector capable of comparing the output of the first frequency divider and the output of the second frequency divider and generating a control signal;

wherein the charge pump is capable of generating the charge pump current based on the control signal.

35. (Previously Presented) The circuit of Claim 34, wherein the phase-frequency detector is capable of generating:

an UP control signal when the output of the first frequency divider is slower than the output of the second frequency divider; and

a DOWN control signal when the output of the first frequency divider is faster than the output of the second frequency divider.

36. (Previously Presented) The circuit of Claim 35, wherein the charge pump is capable of:

injecting the charge pump current into a loop filter when the control signal comprises an UP control signal; and

draining the charge pump current from the loop filter when the control signal comprises a DOWN control signal, the loop filter capable of generating the frequency control voltage level.

37. (Previously Presented) An integrated circuit, comprising:

a processor; and

a phase-locked loop (PLL) frequency synthesizer capable of providing at least one clock signal to the processor, the frequency synthesizer comprising:

a first frequency divider capable of dividing a frequency of an output clock signal based on a first divider value, the output clock signal produced by a voltage controlled oscillator;

a second frequency divider capable of dividing a frequency of a reference clock signal based on a second divider value;

a charge pump capable of generating a charge pump current based on an output of the first frequency divider and an output of the second frequency divider, the charge pump current altering a frequency control voltage level used by the voltage controlled oscillator to generate the output clock signal; and

a loop response control circuit capable of adjusting the charge pump current based at least partially on at least one of: one of a first plurality of ranges in which the first divider value lies and one of a second plurality of ranges in which the second divider value lies.

38. (Previously Presented) A method, comprising:

dividing a frequency of an output clock signal based on a first divider value to produce a first divided signal;

dividing a frequency of a reference clock signal based on a second divider value to produce a second divided signal;

generating a charge pump current based on the first and second divided signals;

altering a frequency control voltage level based on the charge pump current, the frequency control voltage level used to generate the output clock signal; and

adjusting the charge pump current based at least partially on at least one of: one of a first plurality of ranges in which the first divider value lies and one of a second plurality of ranges in which the second divider value lies.